REMARKS

Claims 1, 3-4, 6-12, and 14-30 are pending in the application. Claims 1, 3-4, 6-12, and 14-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins et al, U.S. Patent No. 5,937,436 (hereinafter "Watkins") in view of Horstmann et al, U.S. Patent No. 6,125,433 (hereinafter "Horstmann"), further in view of Futral et al, U.S. Patent No. 5,991,797 (hereinafter "Futral") and further in view of Garcia et al., U.S. Patent No. 6,163,834 (hereinafter "Garcia").

With regard to the Office Action's claim that copendency is not found between the current application and the prior application upon which priority is based, Applicants point to page 1, lines 5-7 of the specification, which make a specific claim for priority based on the provisional application with assigned serial number 60/135,259 filed on May 21, 1999. Moreover, Applicants submit that a reference to the priority provisional application appears on the transmittal letter that accompanied the present application.

With regard to the Office Action's assertion in paragraph 7 that the phrase "a mechanism to flush individual TPT entries..." is unsupported by the provisional application, Applicants respectfully disagree. Support can be found at least at page 26 of the Next Generation I/O Architecture Specification of the provisional application in the paragraph beginning with "Memory de-registration is to the process of invalidating a set of TPT entries...".

Applicants respectfully submit that the cited references do not teach, suggest or disclose at least "[a] host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising: ... a *host-fabric adapter coupled to said processor and provided to interface with said switched fabric*, ... and *protection table (TPT) entries from said host memory*

for a data transaction, each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, ..., a physical page address field to address a physical page frame of data entry, and *a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory...*" (e.g., as described in claim 1).

First, Applicants submit that the Watkins reference does not teach, suggest or disclose a workstation fabric adapter as described in embodiments of the present invention. The Office Action cites to Figure 2A, element 260_K as disclosing a workstation fabric adapter. Applicants disagree. Column 3, lines 40-54 of Watkins disclose element 260_K as being a "microprocessor" (e.g., line 41) or a I/O device (e.g., line 48). Applicants submit a standard microprocessor or I/O device is not the equivalent of a "workstation fabric adapter" as found in embodiments of the present invention, and is therefore inadequate to serve as the basis of a proper rejection. In order to be a proper §103(a) rejection, the cited references must disclose a "workstation fabric adapter" (as described in claimed embodiments of the present application). The Garcia, Horstmann and Futral references fail to disclose the relevant limitation as well. Since features of each of the pending claims are not taught or suggested by the cited references, they are insufficient to support a proper §103(a) rejection and reconsideration and withdrawal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

Next, the Office Action cites column 4, lines 35-50 of Watkins as disclosing protection attributes to control read and write access to a given memory region of said memory. The cited section states:

> A sample physical translation format 281 is also shown in FIG. 2B. In one embodiment, this format 281 includes a valid bit 283, protection bits 285 and the actual physical page bits 287. The valid bit 283, in the descriptor, determines if a specific translation entry will be placed into the ATU (if valid bit 283 is set) or ignored (if valid bit 283 is cleared). *The protection bits 285 are transferred through control line 560 of FIG. 5 in determining whether a page is accessible using the ATU's physical translation for the virtual*

> *address.* For instance, a read-only page can be protected from writes with a read only page protection bit. The physical page bits 287 provide the virtual to physical address mapping for the corresponding portion of the data buffer in virtual address space. The data buffer pointed to by the data buffer pointer 273 can span one or more virtual pages and are not necessarily contiguously placed in physical memory (*emphasis supplied).*

Applicants submit that the cited sections do not teach "...protection attributes to control read and write access to a given memory region of said host memory..." as disclosed in the embodiment of claim 1. The protection bits disclosed in Watkins are directed towards the Watkins ATU or a physical translation unit (see above), *not* towards a memory unit. The Watkins ATU or address translation unit ("ATU"), is described as follows: "an "address translation" is mapping between a virtual address and physical address" (column 1, lines 23-25). Therefore, the protection bits of Watkins are not addressed "...to control read and write access to a given memory region..." as disclosed in embodiments of Applicants' invention, but rather directed toward a temporary mapping feature of Watkins. Therefore, the "protection bits" used in the context of a address translation unit as disclosed in Waltkins are insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

Lastly, the Office Action further asserts that figure 5 and column 4, lines 35-45 of Watkins teaches protection bits are transferred through control lines 560 of Figure 5 while determining whether a page is accessible using the ATU's physical translation for the virtual address and a read only page can be protected from writes with a read-only page protection bit. However, as argued above, regardless of the Office Action's unsupported interpretation of this section, it does not address or describe at all "...a memory protection tag to specify whether said host-fabric adapter has permission *to access said host memory*" as specifically recited in the embodiment of claim 1.

Next, the Office Action asserts that figure 5 and column 7, lines 55 and 60-65 of Watkins teaches the physical address outputting under all condition unless the protection bits 560 signify that the cycle in progress is prohibited due to an attempted write access of a read-only page. Applicants submit that the cited sections only further describe the operation of the ATU, but again do not address or describe at all "...a memory protection tag to specify whether said host-fabric adapter has permission *to access said host memory*" as specifically recited in the embodiment of claim 1.

Applicants submit that since Watkins and indeed, none of the cited references disclose "...a memory protection tag to specify whether said host-fabric adapter has permission *to access said host memory*" as specifically recited in the embodiment of claim 1, the §103(a) rejection should be withdrawn.

Next, the Office Action states that Garcia teaches a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2 lines 20-55). Applicants respectfully disagree and maintain that nowhere in the extensive section cited by the Office Action is the disclosure of a memory protection tag *to specify whether said host fabric adapter has permission to access* a host memory. The reference merely discloses a "protection tag" and states that it is stored in the context memory during the virtual interface creation process.

The Office Action asserts that in column 1, lines 45-55, Garcia teaches that a network interface controller NIC copies data from memory to a network medium and from the medium to the memory. It further asserts that only memory that has been registered with the NIC and Kernel Agent can be used for data transfers. Lastly it asserts Garcia teaches the NIC has access

to the memory protection tags and compares the values to detect invalid accesses of memory. Applicants again maintain regardless of the Office Action's assertions as to the content of these cited sections, none of the cited sections disclose at least a memory protection tag *to specify whether said host fabric adapter has permission to access* a host memory as described in the embodiment of claim 1. Therefore, Applicants further maintain the "protection tag[s]" disclosed in Garcia are again insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

Futral '797 and Horstmann fail to make up for the deficiencies of Garcia and Watkins. Therefore, as shown above, none of at least these argued features are found in the Watkins, Garcia, Futral '797 or Horstmann references taken individually or in combination. Since features of each of the pending claims are not taught or suggested by the cited references, reconsideration and withdrawal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

Conclusion

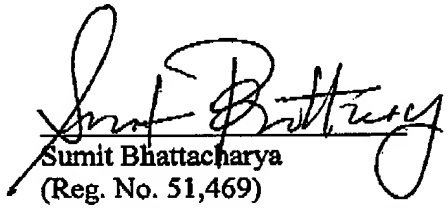
For at least all the above reasons, the Applicants respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: December 27, 2005 By: 

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